



PATENT

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Yates, John S., Jr., et al.

Serial No.: 09/429,094

Art Unit: 2783

Filed: October 28, 1999

Examiner: D. Eng

Title: SIDE TABLES ANNOTATING AN INSTRUCTION STREAM

COMMISSIONER FOR PATENTS

Washington D.C. 20231

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RESPONSE TO OFFICE ACTION OF APRIL 10, 2001

In response to the Office Action of April 10, 2001, please amend the application as follows.

IN THE SPECIFICATION:

On page 62, lines 16-17, replace "the operating system" with --Tapestry operating system

312--.

IN THE CLAIMS:

- 1 1. (twice amended) A microprocessor chip, comprising:
- 2 instruction pipeline circuitry; and
- 3 table lookup circuitry designed to retrieve an entry from [index into] a table, each
- 4 entry of the table being associated with a corresponding address range translated by address
- 5 translation circuitry of the microprocessor chip, each entry describing a likelihood of the
- 6 existence of an alternate coding of instructions located in the respective corresponding
- 7 address range, the table lookup circuitry operable as part of the basic instruction cycle of
- 8 executing an instruction of a non-supervisor mode program executing on a computer;
- 9 interrupt circuitry cooperatively designed with the instruction pipeline circuitry to
- 10 synchronously trigger an interrupt in accordance with interrupt criteria on execution of an

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02 FC:103
03 FC:102

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I certify that this correspondence, along with any documents referred to therein, is being deposited with the United States Postal Service on August 10, 2001 as First Class Mail in an envelope with sufficient postage addressed to The Commissioner for Patents, Washington D.C. 20231.

David E. Boag

Response to Restriction Requirement

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